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Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): Xiuling Li, Paul W. Bohn,  
Jonathan V. Sweedler

For: METAL-ASSISTED CHEMICAL ETCH POROUS  
SILICON FORMATION METHOD

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( ) \_\_\_\_\_ sheet(s) of informal drawing(s).  
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Fee Calculation For Claims As Filed

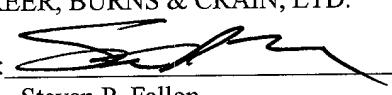
a) Basic Fee		\$ 690.00			
b) Independent Claims	3	- 3	= 0 x	\$ 78.00	= \$ _____
c) Total Claims	21	- 20	= 1 x	\$ 18.00	= \$ 18.00
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# METAL-ASSISTED CHEMICAL ETCH POROUS SILICON FORMATION METHOD

## STATEMENT OF GOVERNMENT INTEREST

4 This invention was made with government assistance from the  
5 Department of Energy under grant FG02 91ER45439. The government has certain  
6 rights in this invention.

## FIELD OF THE INVENTION

The field of the invention is porous silicon formation.

## BACKGROUND OF THE INVENTION

11 Silicon, in its naturally occurring elemental form, is not light  
12 emitting. Silicon may be changed to porous silicon, a modified form of silicon.  
13 The unique electronic, morphological, and thermal properties of porous silicon  
14 make it useful for a range of applications. Porous silicon may even be light  
15 emitting, making it useful in optoelectronics.

16 In addition to potential applications in silicon-based optoelectronics,  
17 porous silicon has been used as an antireflective coating for silicon solar cells.  
18 Chemically modified porous silicon may be useful in chemical and biochemical  
19 sensing. Porous silicon can serve as an efficient matrix for direct introduction of  
20 high mass biomacromolecules in mass spectrometry. In sum, porous silicon is  
21 useful in numerous applications and is likely to find many additional uses in the  
22 future.

23 Conventional methods for producing porous silicon are often time-  
24 consuming, difficult, or ineffective in producing stable porous silicon structures.

1 Equipment such as a potentiostats and illuminating light sources are required in  
2 etching processes of conventional porous silicon production methods. Porous  
3 silicon is normally produced by anodic etching, with (n-type) or without (p-type)  
4 illumination. In the anodic etch process mobile holes are electrically driven to the  
5 silicon-electrolyte interface where they participate in the oxidative dissolution of  
6 surface silicon atoms. Spatial anisotropy results from the potential barrier  
7 developed at the sharp tips of the evolving structures, which block further hole  
8 transport thus preventing further etching and giving rise to the porous structure.  
9 Porous silicon has also been made without external bias by chemical etching in  
10  $\text{HNO}_3/\text{HF}$  solutions (stain etching), and by photochemical etching.

11 Stain etching is typically slow (characterized by an induction  
12 period), inconsistent in result, unreliable in producing light-emitting porous silicon  
13 and is not readily amenable to lateral patterning. Stain etching is mainly used for  
14 making very thin porous silicon layers. Recently, it was shown that evaporating  
15 and annealing 150 – 200 nm of aluminum (Al) on Si results in more rapid stain  
16 etching. However, the porous silicon produced by this aluminum enhanced stain  
17 etching was approximately ten times weaker in luminescence than anodically  
18 etched porous silicon of a similar thickness, and the process still exhibits an  
19 induction period prior to commencement of etching. See, D. Dimova Malinovska  
20 et al., “Thin Solid Films”, 297, 9-12 (1997). It has also been reported that Pt could  
21 be deposited electrochemically from a Pt (IV) solution onto Si during etching to  
22 produce light-emitting porous silicon, although it proved difficult to control the  
23 applied potential to affect both silicon etching and Pt deposition simultaneously.  
24 See, P. Gorostiza, R. Diaz, M. A. Kulandainathan, F. Sanz, and J. R. Morante, J.  
25 *Electroanal. Chem.* 469, 48 (1999).

26 Thus, there is a need for an improved method for forming porous  
27 silicon. It is an object of the invention to meet that need.

## SUMMARY OF THE INVENTION

1                   The present method produces porous silicon (PSi) with tunable  
2 morphologies and light emitting properties. In the method of the invention a thin  
3 discontinuous metal layer is deposited on a silicon surface. Preferred metals are  
4 Pt for strongly light-emitting PSi, Au for PSi with smooth morphology. It is  
5 important that the deposited layer be sufficiently thin that it forms a discontinuous  
6 film, thereby providing access of etchant species to the silicon surface in the area  
7 of the deposited metal. The surface is then etched in a solution including HF and  
8 an oxidant for a brief period, as little as 2 seconds to as much as 60 minutes. A  
9 preferred oxidant is H<sub>2</sub>O<sub>2</sub>. Morphology and light emitting properties of porous  
10 silicon can be selectively controlled as a function of the type of metal deposited, Si  
11 doping type, silicon doping level, and etch time. Electrical assistance is  
12 unnecessary during the chemical etching of the invention.

## BRIEF DESCRIPTION OF THE DRAWINGS

13                   FIG. 1 includes SEM images of Au-coated Si (100) after etching in  
14 HF/H<sub>2</sub>O<sub>2</sub> for 30 s in accordance with the invention. In each image, the top surface  
15 is tilted 30° from normal to reveal both top surface and the cross-section. FIG. 1(a)  
16 is an image of an Au-coated area on p+ Si. FIG. 1(b) is an image taken off the  
17 Au-coated area on p+ Si. FIG. 1(c) is an image taken off the Au-coated area on p-  
18 Si. The scale bars in FIGs. 1(a), 1(b) and 1(c) respectively represent 300 nm, 300  
19 nm and 100 nm.

20                   FIG. 2 includes SEM images of Pt-coated Si (100) after etching in  
21 HF/ H<sub>2</sub>O<sub>2</sub> for 30 s in accordance with the method of the invention. In each image,  
22 the top surface is tilted 30° from normal. FIG. 1(a) is an image of a Pt-coated area  
23 on p+ Si. FIG. 1(b) is an image taken off the Pt-coated area on p+ Si with an inset  
24 showing a high magnification view of the top surface. The scale bars represent 1.2  
25 μm in FIGs. 2(a) and 2(b), respectively, while that of the inset represents 300 nm.

1 FIG. 3 includes top view SEM images of Pt-coated Si (100) after  
2 etching in HF/ H<sub>2</sub>O<sub>2</sub> for 30 s in accordance with the present invention. FIG. 1(a) is  
3 an image of a Pt-coated area of p- Si. FIG. 1 (b) is an image taken off the Pt  
4 coated area of p- Si.

5 FIG. 4 includes luminescence images of p+ and p- Si with patterned  
6 Pt-dots after a 30 s etching in accordance with the invention. The images were  
7 produced in response to excitation at 364 nm and consist of wavelength-integrated  
8 luminescence at wavelengths longer than 400 nm. Due to the limited field of view  
9 only part of the Pt coated dot is shown in the images -- the concave side of the arc  
10 corresponding to the Pt-coated area.

11 FIG. 5 charts photoluminescence spectra taken from Pt-patterned Si  
12 after a 30 s etching in accordance with the invention.

13 FIG. 6 charts the emission spectra of porous silicon samples  
14 prepared from p- silicon by the method of the invention for various etch times,  
15 showing a blue shift of the wavelength of maximum emission with increased etch  
16 time.

17 FIG. 7 charts the x-ray photoelectron spectra of a silicon sample  
18 processed by the method of the invention in the region where Pt was deposited and  
19 in a region away from the Pt deposition, showing that significant Pt remains after  
20 processing.

21 DETAILED DESCRIPTION OF THE INVENTION

22 In the method of the invention, a thin discontinuous layer of metal is  
23 deposited on a Si surface. The surface is then immersed for a short time in an  
24 oxidizing HF solution to produce porous silicon (PSi). The etching reaction may  
25 be carried out in the presence or absence of external illumination, and is conducted  
26 in the absence of external electrical bias. Through the invention, PSi with  
27 different morphologies and luminescence properties can be rapidly produced by  
28 varying: (a) the type of metal deposited, (b) the silicon dopant type, (c) the silicon

1 dopant level, (d) the time of etching, and (e) the amount of metal deposited.  
2 Because much of the metal remains, even after prolonged etching, the invention  
3 may be used to produce PSi with built-in metal contacts, by choosing a metal of  
4 interest for forming ohmic contact to the resulting porous silicon.

5 Samples of PSi have been produced by the invention in laboratory-  
6 scaled experiments. Artisans will recognize the general applicability and  
7 scalability of the invention as a routine extension of the experiments conducted to  
8 demonstrate the invention. In the experiments, silicon (100) wafers with different  
9 doping levels were used, including: p+ (0.01 – 0.03  $\Omega$  cm), p- (1 – 10  $\Omega$  cm), n+  
10 (0.005 – 0.02  $\Omega$  cm) and n- (10 – 20  $\Omega$  cm) Si. 30 – 80  $\text{\AA}$  of metal (Au, Pt, or  
11 Au/Pd) was sputtered onto Si(100), producing metal structures with  $\sim$  10 nm  
12 characteristic lateral dimensions as revealed by atomic force microscopy (AFM).  
13 Removing native oxide from the silicon wafers before sputter coating is not  
14 necessary. Aqueous  $\text{H}_2\text{O}_2$  was added to aqueous HF/EtOH solution in a Teflon  
15 beaker to produce a solution of 1:1:1 EtOH:HF(49%):  $\text{H}_2\text{O}_2$  (30%) immediately  
16 prior to immersing the metal-coated wafers. Etching time can be varied from 2  
17 seconds to 60 min. A mask with rows of 3 mm diameter holes spaced by 6 mm  
18 was used to pattern the metal deposition for comparison of etching and  
19 luminescence properties in the presence and absence of deposited metal. The  
20 development of the pattern deposited using this mask was observed visually upon  
21 immersion in the etching solution, with a color change in the metal-coated region  
22 from gray to brown then to yellow, depending on the elapsed etching time. Gas  
23 evolution from the metal coated area was clearly observed, especially for Pt and  
24 Au/Pd. In no case was any metal dissolution observed, in contrast to the behavior  
25 if thick continuous layers of evaporated Al are deposited prior to etching. A high-  
26 resolution field emission SEM (Hitachi S4700) was used to characterize the  
27 surface morphology, both in-plane and in cross-section. A SPEX fluorimeter  
28 equipped with a 500 W Xe lamp excitation source, two monochromators and a  
29 Hamamatsu RT220P PMT, was used to examine the photoluminescence (PL)

1 spectral behavior. Luminescence images were acquired on an inverted microscope  
2 (Zeiss Axiovert 100) equipped with a 150 W Hg lamp and a color camera (Sony  
3 Medical Instruments, Model DCX 9000).

4 FIGs. 1(a) and 1(b) show SEM images of an Au-coated p+ Si wafer  
5 subjected to HF-oxidant etching for 30 seconds. In FIG. 1(a), large (~ 30 nm)  
6 interconnected pores propagating anisotropically perpendicular to the surface,  
7 similar to the morphology observed on anodically etched PSi from heavily doped  
8 Si, are observed on the Au-coated areas. In contrast, in the areas shown in FIG. 1  
9 between the Au on the same wafer, a much more compact structure with random  
10 arrays of small pores (~ 3 nm spaced by about 3 nm) can be seen, similar to  
11 anodically etched porous silicon from moderately doped (p-) silicon wafers. The  
12 etching depth is about 350 nm and on the Au-coated areas and 250 nm off the Au-  
13 coated areas. For n+ and p- silicon etched under identical conditions, the  
14 morphology in the Au-coated areas exhibits columnar structure similar to the p+  
15 sample seen in FIG. 1(a), with small variations in pore size and etching depth. Off  
16 the Au-coated areas on both n+ and p- silicon the morphology resembles that of p+  
17 samples. A significantly smaller etch depth of 10 nm was obtained for an Au-  
18 coated p- wafer, as seen in FIG. 1(c).

19 The invention was also demonstrated with other metals. FIG. 2  
20 shows SEM images on and off Pt-coated areas of a p+-silicon subjected to HF-  
21 oxidant etching for 30 seconds. The Pt-coated sample results in a rougher and  
22 deeper structure than the Au-coated sample. In the Pt-coated area shown in FIG.  
23 2(a), columnar structures are clustered together at the tip, and the etch depth  
24 exceeds 1  $\mu$ m. The area without Pt shown in FIG. 2(b) is flat with small (~5 – 20  
25 nm) interconnected pores, and the etch depth is 320 nm -- small compared to the  
26 Pt-coated area but deeper than comparable areas on the Au-coated sample. For p-  
27 wafers, the etch depths on and off Pt-coated areas are about 300 nm and 35 nm,  
28 respectively. The p- wafers display smoother top morphology on the Pt-coated  
29 areas, while the off-Pt areas are rougher in depth than those for p+ wafers.

1 HF-oxidant etching of Si coated with Au/Pd in a one-to-one ratio  
2 was also studied. The morphology and luminescence properties of the PSi  
3 produced were similar to Pt-coated Si, as shown by FIG. 3. For all doping  
4 concentrations examined (p+, p- and n+), metal-coated areas always exhibit larger  
5 pores with columnar structure, while the off-metal areas always display smaller  
6 pores (3 – 5 nm) and randomly oriented structures. In each case, the exact pore  
7 sizes and connectivity vary with doping levels and etching time, producing large  
8 differences in luminescence properties.

9 Comparing relative etch rates reveals that Pt-assisted HF-oxidant  
10 etching proceeds much faster than Au-assisted etching. More importantly, PSi  
11 produced with Pt shows more intense photoluminescence (PL) than those  
12 produced by Au-assisted HF-oxidant etching. Furthermore, depending on the  
13 doping type, doping level, and etching time, luminescence patterns can be formed  
14 which are correlated with the metal deposition pattern

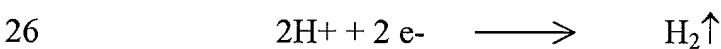
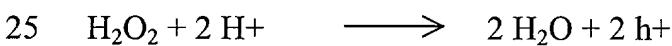
15 FIG. 4 compares luminescence images of HF-oxidant etched p+ and  
16 p- Si patterned with circular Pt areas. Stronger PL can be seen from the Pt-coated  
17 area for p+ wafer, while the uncoated area provides stronger PL in the p- sample.  
18 Stronger PL is also obtained from the Pt-coated areas on n+ Si (not shown). PL  
19 spectra taken from different areas on differently doped samples are shown in FIG.  
20 5. The thin layer (35 nm) in the off Pt areas of p- Si produced the strongest PL  
21 intensity among all samples, and was more intense than 10 times the thickness of  
22 PSi produced by anodic etching. In addition, the PL peaks are centered at 590 nm,  
23 which is blue shifted ~ 100 nm from PSi formed by anodic etching. Furthermore,  
24 with etch times longer than 5 min the resulting material displays a blue-shifted  
25 emission spectrum, with the wavelength of maximum emission scaling with etch  
26 time from 650 nm at 5 min (or shorter) to less than 500 nm at 60 min for p- Si, as  
27 shown in Figure 6.

28 AFM imaging indicates that these thin metal coatings on Si appear  
29 as nanometer size (~ 10 nm) islands prior to etching, with thermal annealing

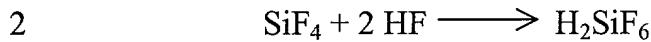
1 producing larger islands. However, the PSi pore sizes produced have no direct  
2 correspondence with the size or spacing of the deposited metal islands, i.e., the  
3 metal-coating does not act as an etch-mask. Etching according to the invention  
4 works not only for p-type Si but also for n-Si, even in the dark. Control  
5 experiments, in which wafers without metal-coatings were immersed for the same  
6 period of time in H<sub>2</sub>O<sub>2</sub>/HF/EtOH, produced no morphological features observable  
7 by SEM and no detectable PL. The results clearly indicate that a thin  
8 discontinuous layer of metal is required for Si etching, with Pt producing the  
9 fastest etching rate and most intensely luminescent PSi. In fact, these metals are  
10 required to obtain chemical etching under the conditions employed here.  
11 Prolonged (up to 60 min) etching of Au-coated Si can produce PSi that is rough  
12 and deep but never as strong in PL as those produced with Pt.

13 Strongly luminescent PSi can also be produced adjacent to, but  
14 macroscopic distances away from, the metal-coated areas, in contrast to control  
15 experiments in which the absence of a metal coating correlates with the lack of  
16 detectable etching. This suggests that lateral transport of charge carriers and  
17 chemical species occurs during etching. Etching by the invention may occur as a  
18 localized electrochemical process, with the nanometer-sized metal acting as a local  
19 cathode. By this model, microscopically local anode (Si) and cathode (metal) sites  
20 form on the etched surface with local cell currents flowing between the sites  
21 during etching. The reaction at the cathode generates holes, while the reaction at  
22 the anode consumes them in the dissolution of Si. In analogy with the pioneering  
23 studies of Si etching, the following mechanism is proposed,

24 Cathode reaction (at metal):



27 Anode reaction:



3      Overall reaction:



5      A critical feature of this reaction scheme is the generation of  $\text{h}^+$  from  $\text{H}_2\text{O}_2$  and  
6      the reduction of  $\text{H}^+$  to form  $\text{H}_2$ , both of which are facilitated by the metal particles.

7      Since  $\text{h}^+$  derives from  $\text{H}_2\text{O}_2$ , this mechanism indicates that PSi can be generated in  
8      the same way regardless of doping type and level, as was observed experimentally.

9      However, the difference in doping level is reflected in the etch depth away from  
10     metal-coated areas. In the uncoated areas, higher doping correlates with faster  
11     etching and deeper etch depths at fixed times. Since the higher conductivity of the  
12      $\text{n}^+$  and  $\text{p}^+$  samples relative to  $\text{p}^-$  samples would facilitate carrier transport, this  
13     observation is also consistent with the above mechanism. The observation of much  
14     higher etch rates for Pt and Pd than Au suggest a catalytic role, but we do not have  
15     direct evidence of catalysis at this time. Finally, the proposed  $\text{H}_2\text{O}_2$  is but one  
16     possible oxidant, and others may work as well or better - the key feature being the  
17     ability to generate mobile holes at the metal-solution interface.

18              Rutherford back scattering analysis and X-ray photoelectron  
19     spectroscopy (FIG. 7) show that some metal remains on the metal coated areas of  
20     the silicon surface after etching by the invention and rigorous rinsing, showing  
21     that etching of the invention should provide in situ metal contacts for PSi. Making  
22     contacts to PSi is important for devices with PSi top layers, because the fragile and  
23     unstable nature of the porous layer makes it difficult to accomplish without  
24     altering the properties of the PSi.

25              While various embodiments of the present invention have been  
26     shown and described, it should be understood that other modifications,  
27     substitutions and alternatives are apparent to one of ordinary skill in the art. Such  
28     modifications, substitutions and alternatives can be made without departing from

1 the spirit and scope of the invention, which should be determined from the  
2 appended claims.

3 Various features of the invention are set forth in the appended  
4 claims.

WHAT IS CLAIMED IS:

1           1. A method for producing porous silicon, the method  
2 comprising steps of:

3           depositing a thin discontinuous layer of metal on a Si surface;

4           etching the Si surface in a HF and oxidant solution, said etching  
5 being conducted without external electrical bias.

1           2. The method according to claim 1, wherein said step of  
2 etching is conducted in the absence of illumination.

1           3. The method according to claim 1, wherein said step of  
2 etching is conducted in the presence of illumination..

1           4. The method according to claim 1, wherein said metal  
2 comprises Pt.

1           5. The method according to claim 1, wherein said metal  
2 comprises Au.

1           6. The method according to claim 1, wherein said metal  
2 comprises Pd.

1           7. The method according to claim 1, wherein said metal  
2 comprises a combination of metals selected from the group of Au, Pt and Pd.

1           8. The method according to claim 1, wherein said oxidant  
2 comprises H<sub>2</sub>O<sub>2</sub>.

1           9. The method according to claim 1, wherein the thickness of  
2 said metal is less than approximately 10nm.

1           10. The method according to claim 1, wherein said etching is  
2 conducted for a time period between about 2 seconds and one hour.

1           11. A method for producing porous silicon, the method consisting  
2 of the following steps:

3           depositing a thin discontinuous layer of metal on a Si surface;

4 etching the Si surface in a HF and oxidant solution for a period of  
5 about two seconds up to 60 minutes, said etching being conducted without  
6 external electrical bias.

1                   12. The method according to claim 11, wherein said step of  
2 etching is conducted in the absence of illumination.

1                   13. The method according to claim 11, wherein said step of  
2 etching is conducted in the presence of illumination.

1 14. The method according to claim 11, wherein said metal  
2 comprises Pt.

1                           15. The method according to claim 11, wherein said metal  
2   comprises Au.

1                           16. The method according to claim 11, wherein said metal  
2   comprises Pd.

1                   17. The method according to claim 11, wherein said metal  
2 comprises a combination of metals selected from the group of Au, Pt and Pd.

1                   18. The method according to claim 11, wherein said oxidant  
2   comprises  $\text{H}_2\text{O}_2$ .

1 19. The method according to claim 11, wherein the thickness of  
2 said metal is less than approximately 10nm.

1                   20. The method according to claim 11, wherein said etching is  
2 conducted for a time period between about 2 seconds and one hour.

1                   21. A method for producing porous silicon, the method  
2 comprising steps of:

3 depositing metal on a Si surface in a thickness sufficient to permit  
4 nucleation that forms nanometer size metal particles and small enough to prevent  
5 formation of a continuous metal layer;

6 etching the Si surface in a HF and oxidant solution for a period of  
7 about two seconds up to 60 minutes, said etching being conducted without  
8 external electrical bias.

## ABSTRACT

2 A thin discontinuous layer of metal such as Au, Pt, or Au/Pd is  
3 deposited on a silicon surface. The surface is then etched in a solution including  
4 HF and an oxidant for a brief period, as little as a couple seconds to one hour. A  
5 preferred oxidant is H<sub>2</sub>O<sub>2</sub>. Morphology and light emitting properties of porous  
6 silicon can be selectively controlled as a function of the type of metal deposited, Si  
7 doping type, silicon doping level, and/or etch time. Electrical assistance is  
8 unnecessary during the chemical etching of the invention, which may be  
9 conducted in the presence or absence of illumination.

Fig. 1

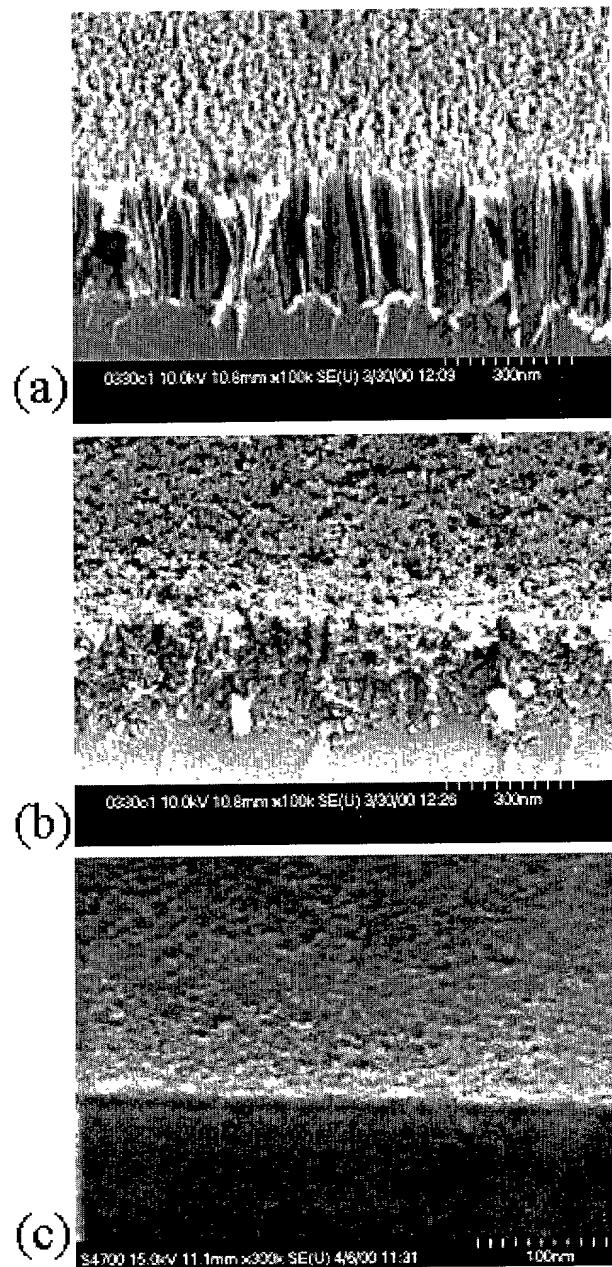


Fig. 2

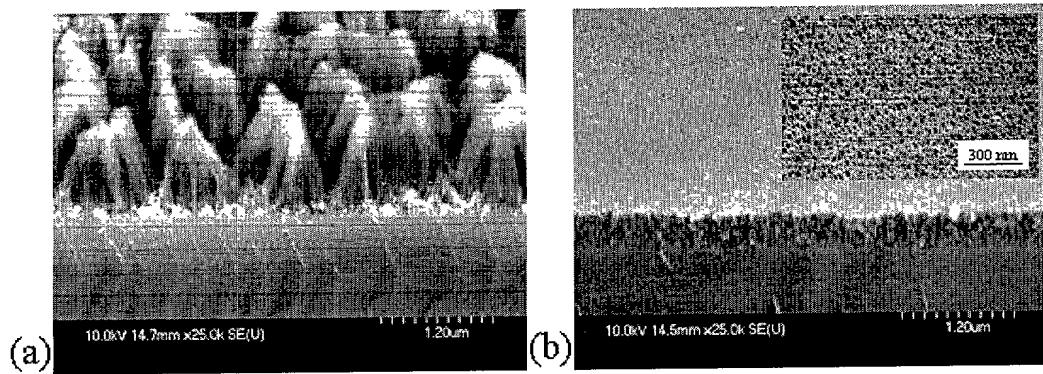


Fig. 3

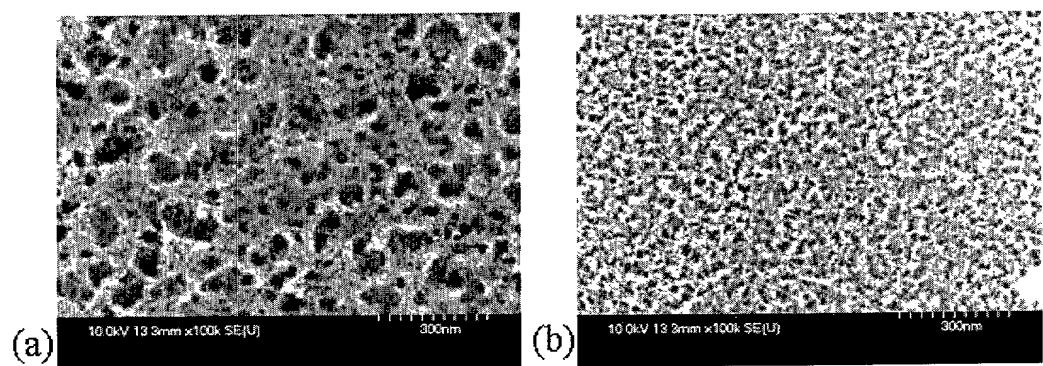


Fig. 4

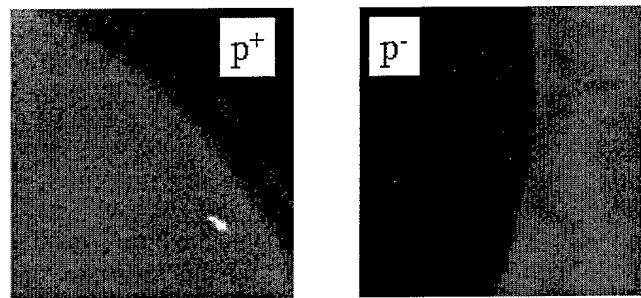


Fig. 5

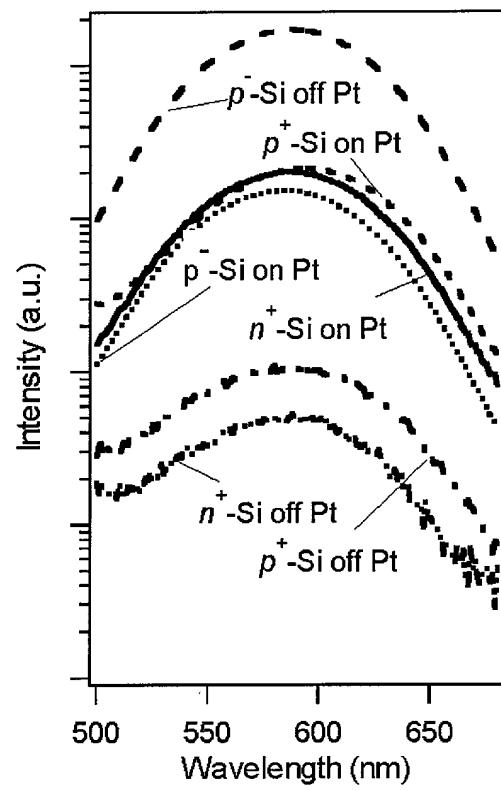


Fig. 6

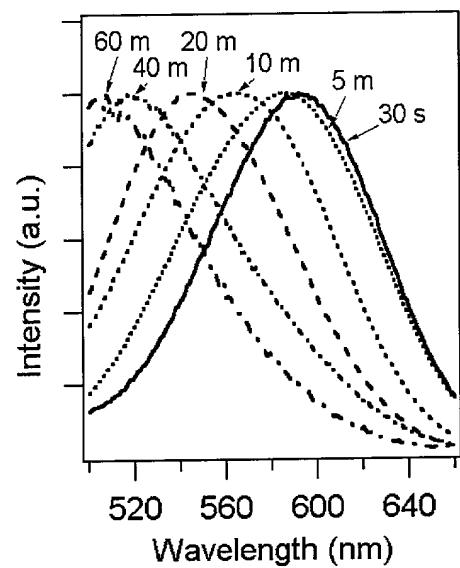
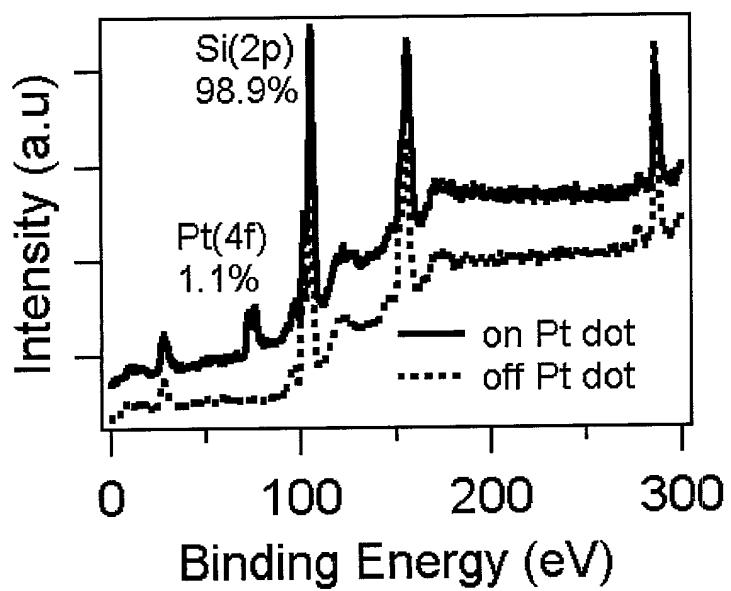


Fig. 7



**DECLARATION AND POWER OF ATTORNEY**

As a below named inventor, I hereby declare:

That my residence, post office address and citizenship are as stated below next to my name.

That I verily believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**METAL-ASSISTED CHEMICAL ETCH POROUS SILICON FORMATION METHOD**

the specification of which (check one)

is attached hereto.

was filed on \_\_\_\_\_  
Application Serial No. \_\_\_\_\_  
and was amended on \_\_\_\_\_  
(if applicable)

That I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

That I acknowledge the duty to disclose information known to be material to patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

That I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate on this invention having a filing date before that of the application on which priority is claimed:

<b>Prior Foreign Application(s)</b>			<b>Priority Claimed</b>
<hr/> <input type="checkbox"/> (Number)	<hr/> <input type="checkbox"/> (Country)	<hr/> <input type="checkbox"/> (Day/Month/Year Filed)	<input type="checkbox"/> ( ) Yes <input type="checkbox"/> ( ) No
<hr/> <input type="checkbox"/> (Number)	<hr/> <input type="checkbox"/> (Country)	<hr/> <input type="checkbox"/> (Day/Month/Year Filed)	<input type="checkbox"/> ( ) Yes <input type="checkbox"/> ( ) No
<hr/> <input type="checkbox"/> (Number)	<hr/> <input type="checkbox"/> (Country)	<hr/> <input type="checkbox"/> (Day/Month/Year Filed)	<input type="checkbox"/> ( ) Yes <input type="checkbox"/> ( ) No

That I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

**United States Application(s)**

<hr/> <input type="checkbox"/> (Application Serial No.)	<hr/> <input type="checkbox"/> (Filing Date)	<hr/> <input type="checkbox"/> (Status)-(Patented, pending, abandoned)
<hr/> <input type="checkbox"/> (Application Serial No.)	<hr/> <input type="checkbox"/> (Filing Date)	<hr/> <input type="checkbox"/> (Status)-(Patented, pending, abandoned)
<hr/> <input type="checkbox"/> (Application Serial No.)	<hr/> <input type="checkbox"/> (Filing Date)	<hr/> <input type="checkbox"/> (Status)-(Patented, pending, abandoned)

That all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

I hereby appoint the following attorneys and agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith and request that all correspondence and telephone calls in respect to this application be directed to GREER, BURNS & CRAIN, LTD., Suite 8660 - Sears Tower, 233 South Wacker Drive, Chicago, Illinois 60606, Telephone No. (312) 993-0080:

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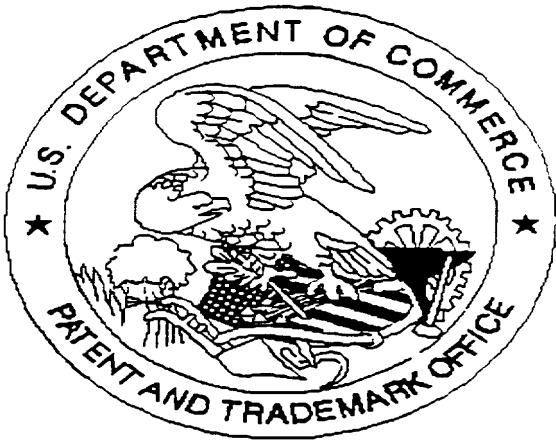
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